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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,102	08/22/2003	Michael Bryndzia	905P181A	8415

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EXAMINER

DOLE, TIMOTHY J

ART UNIT PAPER NUMBER

2858

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,102	BRYNDZIA ET AL.	
	Examiner	Art Unit	
	Timothy J. Dole	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 March 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 and 25-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21, 23, 25 and 33-40 is/are rejected.
- 7) ☒ Claim(s) 22 and 26-32 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10, 19-21, 25 and 33-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Brownell.

Referring to claim 1, Brownell discloses an electric circuit test device for testing an electric circuit, the test device being insertable in a receptacle, the receptacle including electrical terminals coupled to the electrical circuit, the device comprising: a housing (fig. 15 (118)) characterized by a longitudinal axis; a plug blade (fig. 16 (146)) assembly disposed within the housing and configured to mate with the electrical terminals (fig. 16), electrical continuity being established between the plug blade assembly and the electric circuit (column 15, lines 51-54); a fault detection circuit (fig. 14) coupled to the plug blade assembly and disposed within the housing, the fault detection circuit being configured to detect a circuit status condition in the electrical circuit (column 6, lines 42-43); and at least one circuit status indicator assembly (fig. 15) coupled to the fault detection circuit and normal thereto, the at least one circuit status indicator assembly including a plurality of semiconductor light indicators (fig. 15 (124), (126) and (128)) connected substantially normal to the at least one circuit status indicator assembly, the

plurality of semiconductor light indicators being configured to emit a code corresponding to the circuit status condition in a direction normal to the longitudinal axis with a viewing angle less than approximately 30° (column 14, lines 54-57). It should be noted that since the semiconductor light indicators of Brownell are LED's, their viewing angle would be less than 30°.

Referring to claim 2, Brownell discloses the device as claimed wherein the fault detection circuit is configured to detect the circuit status condition in a single-phase grounded neutral electric circuit (column 11, lines 55-58).

Referring to claim 3, Brownell discloses the device as claimed wherein the circuit status condition includes an open hot wire status condition (column 12, line 24).

Referring to claim 4, Brownell discloses the device as claimed wherein the circuit status condition includes an open neutral wire status condition (column 12, lines 15-16).

Referring to claim 5, Brownell discloses the device as claimed wherein the circuit status condition includes an open ground status condition (column 12, lines 17-18).

Referring to claim 6, Brownell discloses the device as claimed wherein the circuit status condition includes a hot/neutral reversed polarity status condition (column 12, lines 19-20).

Referring to claim 7, Brownell discloses the device as claimed wherein the circuit status condition includes a properly wired and grounded status condition (column 12, line 14).

Referring to claim 8, Brownell discloses the device as claimed wherein the fault detection circuit includes a mis-wire protection circuit portion, the mis-wire protection

circuit portion prevents component destruction during a mis-wire condition, such that the device is operable after the mis-wire condition (column 12, lines 7-11).

Referring to claim 9, Brownell discloses the device as claimed wherein the mis-wire protection circuit portion includes at least one diode component inhibiting reverse biased current (column 12, lines 7-11).

Referring to claim 10, Brownell discloses the device as claimed wherein the single phase grounded neutral electric circuit supports 120 VAC, 277 VAC, or 347 VAC (fig. 12 see box on lower left-hand side).

Referring to claim 19, Brownell discloses the device as claimed wherein the code emitted by the at least one circuit status indicator assembly is a Boolean code (fig. 15).

Referring to claim 20, Brownell discloses the device as claimed wherein the plurality of semiconductor light indicators further comprises a plurality of LED elements (fig. 15 (124), (126) and (128)) coupled to the fault detection circuit by way of a circuit board standoff element, the plurality of LED elements being configured to display the code (column 14, lines 54-57).

Referring to claim 21, Brownell discloses the device as claimed wherein the plurality of LED elements comprise LEDS of a different color (column 9, lines 36-37).

Referring to claim 25, Brownell discloses an electric circuit test device for testing an electric circuit, the test device comprising: a housing (fig. 9 (48)) characterized by a longitudinal axis; a connector cable (fig. 9) coupled to the electric circuit and to the housing (column 10, line 66 – column 11, line 2); electrical terminals (fig. 9 (50)) coupled to the connector cable, electrical continuity being established between the

electrical terminals and the electric circuit (column 11, lines 1-2); a fault detection circuit (fig. 2) coupled to the electrical terminals (fig. 2) and disposed within the housing (column 10, lines 66-67), the fault detection circuit being configured to detect a circuit status condition in the electrical circuit and connector cable (column 7, line 55 – column 8, line 5); and at least one circuit status indicator assembly (fig. 12) coupled to the fault detection circuit and normal thereto, the at least one circuit status indicator assembly including a plurality of semiconductor light indicators (fig. 2 (L1-L3)) connected substantially normal to the at least one circuit status indicator assembly, the plurality of semiconductor light indicators being configured to emit a code corresponding to the circuit status condition in a direction normal to the longitudinal axis with a viewing angle less than approximately 30° (column 7, line 55 – column 8, line 5). It should be noted that since the semiconductor light indicators of Brownell are LED's, their viewing angle would be less than 30°.

Referring to claims 33 and 36, Brownell discloses the device as claimed wherein the circuit status condition includes an open hot wire condition (column 7, lines 57-58).

Referring to claim 34, Brownell discloses the device as claimed wherein the circuit status condition includes an open ground status condition (column 7, lines 59-60).

Referring to claim 35, Brownell discloses the device as claimed wherein the circuit status condition includes a hot and ground reversed status condition (column 8, lines 2-3).

Referring to claim 37, Brownell discloses the device as claimed wherein the circuit status condition includes a properly wired and grounded status condition (column 7, line 64).

Referring to claim 38, Brownell discloses the device as claimed wherein the fault detection circuit is configured to detect the circuit status condition in a single-phase grounded neutral electric circuit (column 7, lines 30-33).

Referring to claim 39, Brownell discloses the device as claimed wherein the single phase grounded neutral electric circuit supports 120 VAC, 277 VAC, or 347 VAC (fig. 12 see box on lower left-hand side).

3. Claims 1, 13-18 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Roveti.

Referring to claim 1, Roveti discloses an electric circuit test device for testing an electric circuit, the test device being insertable in a receptacle, the receptacle including electrical terminals coupled to the electrical circuit, the device comprising: a housing (fig. 1 (11)) characterized by a longitudinal axis; a plug blade (fig. 1 (12-14)) assembly disposed within the housing and configured to mate with the electrical terminals (fig. 1 (15-17)), electrical continuity being established between the plug blade assembly and the electric circuit (column 2, lines 45-49); a fault detection circuit (fig. 4) coupled to the plug blade assembly and disposed within the housing, the fault detection circuit being configured to detect a circuit status condition in the electrical circuit (column 4, lines 11-14); and at least one circuit status indicator assembly (fig. 4) coupled to the fault detection circuit and normal thereto, the at least one circuit status indicator assembly

including a plurality of semiconductor light indicators (fig. 1 (23-25)) connected substantially normal to the at least one circuit status indicator assembly, the plurality of semiconductor light indicators being configured to emit a code corresponding to the circuit status condition in a direction normal to the longitudinal axis with a viewing angle less than approximately 30° (column 4, lines 8-11). It should be noted that since the semiconductor light indicators of Roveti are LED's (column 4, lines 67-68), their viewing angle would be less than 30° .

Referring to claims 13 and 24, Roveti discloses the device as claimed wherein the fault detection circuit is configured to detect the circuit status condition in a multi-phase center grounded electric circuit (column 4, lines 45-51).

Referring to claims 14 and 17, Roveti discloses the device as claimed wherein the circuit status condition includes an open hot wire condition (column 4, lines 56-62). It should be noted that if the hot wire were open, no lights would be illuminated.

Referring to claim 15, Roveti discloses the device as claimed wherein the circuit status condition includes an open ground status condition (column 4, lines 56-58).

Referring to claim 16, Roveti discloses the device as claimed wherein the circuit status condition includes a hot and ground reversed status condition (column 4, lines 48-61).

Referring to claim 18, Roveti discloses the device as claimed wherein the circuit status condition includes a properly wired and grounded status condition (column 4, lines 53-54).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 11, 12 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brownell in view of Kusko et al.

Referring to claim 11, Brownell discloses the device as claimed wherein the fault detection circuit includes a redundant ground current safety portion (column 12, lines 3-7).

Brownell does not disclose that the redundant ground current safety portion prevents ground current from exceeding 500 microamperes.

Kusko et al. discloses a fault detection circuit with a redundant ground current safety portion that prevents ground current from exceeding 500 microamperes (column 6, lines 19-21).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the current limitations of Kusko et al. into the device of Brownell for the purpose of specifying limitations whereby disclosing a safer circuit for protecting against ground current.

Referring to claim 12, Brownell discloses the device as claimed wherein the ground current safety portion includes a plurality of resistors in series (fig. 14 (R1-R3) and (R5-R7)).

Referring to claim 40, Brownell discloses the device as claimed, except wherein the fault detection circuit is configured to detect the circuit status condition in a multi-phase center grounded electric circuit.

Kusko et al. discloses the fault detection circuit is configured to detect the circuit status condition in a multi-phase center grounded electric circuit (column 17, lines 1-3).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the configuration of Kusko et al. into the device of Brownell for the purpose of being able to detect a wider variety of circuit configurations whereby making the device more universal.

6. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brownell in view of Brown.

Referring to claim 23, Brownell discloses the device as claimed except for an acoustic device configured to emit the circuit status condition.

Brown discloses a fault detector including an acoustic device configured to emit the circuit status condition (abstract).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the acoustic device of Brown into the device of Brownell for the purpose of providing additional indication of a fault condition whereby leading to a more reliable system.

Allowable Subject Matter

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7. Claims 22 and 26-32 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed March 16, 2005 have been fully considered but they are not persuasive.

9. In response to Applicants arguments with respect to claim 1, that "the Examiner does not point out where Brownell discloses a "circuit status indicator assembly coupled to the fault detection circuit and normal thereto," as recited in claim 1." and "The Examiner also does not show where Brownell discloses a plurality of semiconductor light indicators being connected substantially normal to the circuit status indicator assembly" (page 3, lines 6-10), it should be noted that as stated in the above rejection, the semiconductor light indicators are shown in fig. 15 as 124, 126 and 128 as part of the circuit status indicator assembly which also includes display panel 122. As seen from fig. 15, the semiconductor light indicators are normal to the display panel and are also part of the display panel, so therefore the semiconductor light indicators are included in the circuit status indicator assembly and are also normal to it. The circuit status indicator assembly is coupled to the fault detection circuit and normal thereto since the semiconductor light indicators are part of the circuit status indicator assembly and are also normally connected to the fault detection circuit.

10. In response to Applicants arguments with respect to claims 8 and 9, that "the Examiner does not show where Brownell anticipates either claim 8 or claim 9" (page 3, lines 18-19), it

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should be noted that as stated in the above rejection, Brownell discloses diodes inhibiting reverse biased current (column 12, lines 7-8). The diodes of Brownell may be referred to as a mis-wire protection circuit since mis-wiring causes reverse biasing and the diodes of Brownell are provided for the purpose of preventing reverse biasing. Applicants seem to have misunderstood the Brownell reference by thinking that the diode “prevents reverse biasing of the LEDs if the line voltages are *less than a predetermined amount*” (page 3, lines 16-17). A proper reading of Brownell shows that the diodes prevent reverse biasing of the LEDs, while separate components called sidacs function as switches to prevent LEDs from operating with line voltages from the hot conductor of less than a predetermined amount (column 12, lines 7-11).

11. In response to Applicants arguments with respect to claims 10 and 39, that “the Examiner does not show where Brownell discloses the subject matter of claim 10” (page 3, lines 22-23), it should be noted that as stated in the above rejection, Brownell shows the device supports a rating of 120 VAC (fig. 12). Claim 10 simply recites the limitation that the circuit support 120 VAC, 277 VAC OR 347 VAC (emphasis added). Since the Brownell device discloses 120 VAC, it reads over the limitations of claim 10.

12. In response to Applicants arguments with respect to claim 19, that “the Examiner does not show where Brownell discloses the subject matter of claim 19” (page 3, lines 28-29), it should be noted that as stated in the above rejection, Brownell discloses that the LEDs are lit in certain combinations, the different possible conditions are displayed (column 12, lines 12-27). For example if L1 AND L3 are lit and NOT L2, then there is correct wiring. These AND and NOT combinations of lit LEDs provide a Boolean code that is compared to display 122 in fig. 15 to determine the condition of the conductors.

13. In response to Applicants arguments with respect to claim 20, that “the Examiner does not show where Brownell discloses the subject matter of claim 20” (page 4, lines 2-3), it should be noted that the LEDs of Brownell are shown coupled to the fault detection circuit in fig. 14. In fig. 15 the LEDs are shown as coming through the housing 118 so as to be part of the display panel 122. Therefore, the LEDs must be connected to the fault detection circuit by an element such as the LED’s contact leads, which are considered to be the circuit board standoff elements.

14. In response to Applicants arguments with respect to claim 25, “the Examiner fails to show where Brownell discloses a “circuit status indicator assembly coupled to the fault detection circuit and normal thereto,” as recited in claim 25.” and “The Examiner also does not show where Brownell discloses a plurality of semiconductor light indicators being connected substantially normal to the circuit status indicator assembly” (page 4, lines 10-13), it should be noted that as stated in the above rejection, the semiconductor light indicators are shown in fig. 2 as L1-L3 as part of the circuit status indicator assembly which also includes display panel 58 in fig. 9, which can be replaced by 62 in fig. 10. As seen from fig. 10, the semiconductor light indicators 1-3 are normal to the display panel and are also part of the display panel, so therefore the semiconductor light indicators are included in the circuit status indicator assembly and are also normal to it. The circuit status indicator assembly is coupled to the fault detection circuit and normal thereto since the semiconductor light indicators are part of the circuit status indicator assembly and are also normally connected to the fault detection circuit.

15. In response to Applicants arguments with respect to the rejection of claim 1 by Roveti (page 5, lines 11-15), it should be noted that the circuit status indicator assembly is made up of signal lights 23-25 and the end of housing 11. Therefore, the signal lights are normal to the

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circuit status indicator assembly. The fault detection circuit shown in fig. 4 is mounted on circuit board 44 in fig. 3, and is therefore normal to the circuit status indicator assembly.

16. In response to Applicants arguments with respect to claims 13 and 24, that “the Examiner does not show where Brownell discloses the subject matter of claim 13 or claim 24” (page 5, lines 24-25), it should first be noted that the rejection is with respect to Roveti not Brownell as argued. Secondly, Roveti is giving examples of electrical systems with which the tester will work. Column 4 of Roveti goes on to disclose the light combinations that will be seen in different wiring situations, for example, if the wiring is correct, lights 23 and 25 will light (column 4, lines 53-54). Therefore the above cited passage is relevant to Roveti’s invention for explaining the light patterns that can be expected.

17. In response to Applicants arguments with respect to claim 11, that “Kusko does not supply the missing claim elements” (page 6, lines 31-32), it should be noted that Kusko discloses “a ground loop current on the order of 150 microamperes, which may be further reduced if desired by altering resistor values” (column 6, lines 19-21). Therefore Kusko, by controlling resistor values, can control the ground loop current to be around 150 microamperes, which is well below the claimed limit of 500 microamperes.

Final Rejection

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event; however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

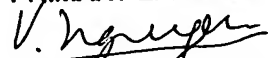
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Dole whose telephone number is (571) 272-2229.

The examiner can normally be reached on Mon. thru Fri. from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571) 272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJD

VINCENT Q. NGUYEN
PRIMARY EXAMINER
6/01/2005